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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/029,709	TANG ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-38 and 41-45* is/are rejected.

7)☒ Claim(s) *39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 34 and 37-45 are objected to because of the following informalities:

In claim 34, line 1, "claim 33" should be "claim 32" to avoid the conflict of claim 33 since claim 33 already recites the detector is a binary phase detector.

In claim 37, line 3, "a phase shift in said PL" should be "the phase shift in said PLL".

In claim 38, line 7, "and output signal" should be "output signals".

In claim 39, both lines 7 and 9, "an input signal" should be "input signals".

In claim 38 (line 8) and claim 39 (lines 9-10), "said read counter" should be "said read counter to generate the fill level" since both claims 38 and 39 lack connection of cooperation with the precedent claim 30.

In claim 40, lines 8-9, "an input from said counters and said FIFO register and also providing an output to said FIFO register and" should be "input signals from both said write counter and said read counter and providing output signals".

In claim 40, lines 9-10, "said binary decoder" should be "said binary decoder to generate the fill level" since claim 40 also lacks connection of cooperation with the precedent claim 30.

In claim 41, lines 3 and 4, "FIFO" should be "FIFO register".

In line 2 of both claims 42 and 44, "claim 40" should be "claim 41" since claim 40 is an apparatus claim.

In claim 43, line 2, "with" should be "in".

In claim 44, line 2, "a local reference clock" should be "the local reference clock". Wherein claim 45 depends upon claim 44.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 34 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to support the claim subject matter that the detector output from the FIFO register is a wide band phase detector as recited in the new claim 34.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 30-38 and 41-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu (US Patent No. 6,901,126) in view of Applicants Admitted Prior Art (hereinafter "AAPA") and/or Rude (US Patent No. 6,415,006).

Regarding claims 30, 32, 35, 38, 41-42 and 44, Gu discloses a dual loop synchronization system in Figure 3 or method comprising a phase lock loop (PLL) 30 and a delayed lock loop (DLL) 32. The PLL 30 comprises a phase/frequency detector (PFD) 34, a loop filter 36, a voltage controlled oscillator (VCO) 38, and a frequency divider 46. The DLL 32 comprises a data recovery circuit 40 including a phase detector in well known manner (not shown), a phase select circuit/filter 42, and a phase interpolator 44 (phase shifter) coupled to the VCO 38 configured in a feedback loop with the PFD, and receiving a local reference clock signal REFCLK, wherein the phase selector circuit/filter (digital loop filter) is coupled between the data recovery circuit 40 (phase detector) and the phase interpolator 44 to produce a phase shift to the PLL 30. See column 3, line 35 to column 5, line 59. Although Gu does not explicitly show or

suggest that the input data of the data recovery circuit 40 is input from a first-in first-out (FIFO) register receiving a parallel data input for detecting the fill level of the FIFO.

However, as admitted in the AAPA described in the Background of the Invention and shown in Figures 1-4, PLLs and DLLs are common systems used in the input/output interfaces of data communication systems, such as, a synchronization circuit comprises an elastic FIFO buffer, a write counter, and a read counter, wherein the FIFO buff outputs parallel input signals to a DLL and a PLL in order to generate a synchronization signal or clock signal to the write and read counters.

Rule also discloses a synchronization circuit in Figure 3 as described in the AAPA comprises an elastic FIFO buffer 14, a write counter 20, a read counter 22, wherein the FIFO buffer outputs parallel input signals to a phase comparator 24 of a DLL (24, 26, 28, 33), the output of which controls a PLL (24, 34, 36, 22) to control the clock of the read counter 22.

Therefore, it would have been obvious to one of ordinary skill in the art as taught by either AAPA or Rude to include a FIFO buffer in Gu's time division multiplex data recover system in order to temporary store the input data first before releasing the fill level of the input data to the phase detector of the data recovery circuit 40 for the purpose of synchronizing input data by the sampling clock and the leading clock generated from the VCO 38 of the PLL 30.

Regarding claims 30 and 31, although the phase interpolator (phase shifter) 44 is integrated in the DLL instead of the PLL and the PLL 30 is not embedded in the DLL. It is well known to a person skill in the art to embed or integrate the phase interpolator 44

into the PLL for the same purpose of generating a phase shift feedback signal to the frequency/phase detector of the PLL and embed or integrate both the PLL and the DLL into one integrate circuit in order to have a smaller device for storage or save money.

Regarding claim 33, the phase detector 24 is a digital phase detector and receives binary signals from the elastic storage circuit 14. Therefore, the phase detector 24 is a binary phase detector.

Regarding claims 34, 36-37, 43 and 45, as admitted in AAPA, the phase detector 407 and the digital loop filter 408 of Figure 4 can be operated in narrow or wide band which depends on the operating frequency range of the PLL bandwidth.

Allowable Subject Matter

7. Claims 39 and 40 would be allowable if rewritten to overcome the objection(s) set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YOUNG T. TSE
Primary Examiner
Art Unit 2611